AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace the Abstract with the following amended Abstract:

A self-testing and correcting ~~read only~~ random access memory (RAM) device and methodology is disclosed herein. The device includes at least one array of memory to enable data storage and self-testing RAM interface for evaluating, correcting, and/or compensating for memory cell errors. The RAM device, *via* the self-testing RAM interface, supports interaction with a central processing unit (CPU) to facilitate testing of the CPU to memory interface as well as the device memory array. Upon detection of memory errors, the self-testing RAM interface can notify the CPU, notify an exception handler, correct, and/or compensate for the errors. Error correction can be accomplished using error correction codes (ECCs) alone or in combination with retrieval and replacement of erroneous data with correct data stored in different locations. Memory cells that are physically defective and incapable of maintaining data integrity can be compensated for by mapping defective cells to a plurality of reserved replacement cells.

SD 10/15/07

Please replace the paragraph at page 10 lines ~~21 – page 11 line 2~~ 17 with the following amended paragraph.

Self-testing RAM interface 122 in accordance with an aspect of the subject invention can be employed as a virtual memory manager and a memory paging mechanism. Accordingly, it should be noted that during initial system startup while self-testing RAM interface 122 is testing the memory of memory store 344, self-testing RAM interface 122 can map all address/data accesses by the CPU [[302]] 110 to memory cells provided by memory stores 340 and [[343]] 342 which are not in the process of being tested. Thus, the actual amount of physical storage may therefore increase moments after system startup as the additional memory stores come online. Self-testing RAM interface 122 can also perform RAM cell testing without CPU [[302]] 110 interventions by mapping all present live data and address line 304 and data bus 306 access to memory stores 340 and 342 while using self-testing RAM interface 122 to test the memory cells such as cell 354 in memory store 344.